Flash FPGAs

Flash SoC FPGAs

Military FPGAs

Automotive FPGAs

Ecosystem

Design Hardware

Intellectual Property

Technology Solutions

Microsemi®

Power Matters.™

Microsemi

Power Matters.™

Delivering More Resources in Low Density Devices with the Lowest Power, Proven Security and Exceptional Reliability

Microsemi FPGAs & SoC FPGAs

Whether you're designing at the board or system-level, **Microsemi's SoC FPGAs and low-power FPGAs are your best choice.** The unique, flash-based technology of Microsemi FPGAs, coupled with their history of reliability, sets them apart from traditional FPGAs.

Design for today's rapidly growing markets of consumer and portable medical devices, or tomorrow's environment friendly data centers, industrial controls and military and commercial aircraft. Only Microsemi can meet the power, size, cost and reliability targets that reduce time-to-market and enable long-term profitability.

Table of Contents

Refer to www.microsemi.com/fpga-soc and corresponding product datasheets for the latest device information, valid ordering codes and more information regarding previous generations of flash FPGAs.

SmartFusion2 SoC FPGAs

More resources in low density devices with ARM Cortex-M3 processor

SmartFusion2 SoC FPGAs deliver more resources in low density devices, with the lowest power, proven security and exceptional reliability. These devices are ideal for general purpose functions such as Gigabit Ethernet or dual PCI Express control planes, bridging functions, input/output (I/O) expansion and conversion, video/image processing, system management and secure connectivity. Microsemi SoC FPGAs are used by customers in Communications, Industrial, Medical, Defense, and Aviation markets.

- Embedded ARM Cortex-M3 Microcontroller Subsystem
- PCIe Gen2 endpoints starting at 10 K Logic Elements
- Embedded DDR3 memory controllers
- Small packages
- 1 mW in Flash*Freeze mode
- Instant-on
- Zero FIT FPGA Configuration Cells
- SECDED memory protection
- NRBG, AES-256, SHA-256, ECC Cryptographic Engine
- User Physically Unclonable Function (PUF)
- CRI DPA Pass through license

SmartFusion2 Devices

SmartFusion2 Devices	Features	M2S005	M2S010	M2S025	M2S050	M2S060	M2S090	M2S150
Logic/DSP	Maximum Logic Elements (4LUT + DFF)	6,060	12,084	27,696	56,340	56,520	86,184	146,124
	Mathblocks (18 x 18)	11	22	34	72	72	84	240
	Fabric Interface Controllers (FICs)	1	1	1	2	1	1	2
	PLLs and CCCs	2	2	2	6	6	6	8
	Security	AES256, SHA256, RNG	AES256, SHA256, RNG	AES256, SHA256, RNG	AES256, SHA256, RNG	AES256, SHA256, RNG, ECC, PUF	AES256, SHA256, RNG, ECC, PUF	AES256, SHA256, RNG, ECC, PUF
MSS	Cortex-M3 + instruction Cache	Yes						
	eNVM (K Bytes)	128	256	256	256	256	512	512
	eSRAM (K Bytes)	64						
	eSRAM (K Bytes) Non-SECDED	80						
	CAN, 10/100/1000 Ethernet, HS USB	1 each						
	Multi-Mode UART, SPI, I^{2}C, Timer	2 each						
Fabric Memory	LSRAM 18 K Blocks	10	21	31	69	69	109	236
	uSRAM 1 K Blocks	11	22	34	72	72	112	240
	Total RAM (K bits)	191	400	592	1,314	1,314	2,074	4,488
High-Speed	DDR Controllers (count × width)	1×18	1×18	1×18	2×36	1×18	1×18	2x36
	SERDES Lanes	0	4	4	8	4	4	16
	PCIe End Points	0	1	1	2	2	2	4
User I/O	MSIO (3.3 V)	115	123	157	139	271	309	292
	MSIOD (2.5 V)	28	40	40	62	40	40	106
	DDRIO (2.5 V)	66	70	70	176	76	76	176
	Total User I/Os	209	233	267	377	387	425	574

I/Os Per Package

	Package Options																		
Package Type	FCS(G)325		VF(G)256		FCS(G)536		VF(G)400		FCV(G)484		TQ(G)144		FG(G)484		FG(G)676		FG(G)896		FC(G)1152
Pitch (mm)	0.5		0.8		0.5		0.8		0.8		0.5		1.0		1.0		1.0		1.0
Length x Width (mm)	11x11		14x14		16x16		17x17		19x19		20x20		23x23		27x27		31x31		35x35
Device	I/O	Lanes	I/O	Lanes	I/O	Lanes	I/O	Lanes	I/O	Lanes	I/O	Lanes	I/O	Lanes	I/O	Lanes	I/O	Lanes	I/O	Lanes
M2S005 (S)	—	—	161	—	—	—	171	—	—	—	84	—	209	—	—	—	—	—	—	—
M2S010 (S/T/TS)	—	—	138	2	—	—	195	4	—	—	84	—	233	4	—	—	—	—	—	—
M2S025 (T/TS)	180	2	138	2	—	—	207	4	—	—	—	—	267	4	—	—	—	—	—	—
M2S050 (T/TS)	200	2	—	—	—	—	207	4	—	—	—	—	267	4	—	—	377	8	—	—
M2S060 (T/TS)	200	2	—	—	—	—	207	4	—	—	—	—	267	4	387	4	—	—	—	—
M2S090 (T/TS)	180	4	—	—	—	—	—	—	—	—	—	—	267	4	425	4	—	—	—	—
M2S150 (T/TS)	—	—	—	—	293	4	—	—	248	4	—	—	—	—	—	—	—	—	574	16

Notes:
1. M2S090 FCSG325 package dimension is 11x13.5.
2. Highlighted devices can migrate vertically in the same package.
3. (G) indicates that the package is RoHS 6/6 Compliant/Pb-free.

www.microsemi.com/products/fpga-soc/soc-fpga/smartfusion2

IGLOO2 FPGAs

More resources in low density devices with High Performance Memory Subsystem

Microsemi's IGLOO2 FPGAs deliver more resources in low density devices, with the lowest power, proven security and exceptional reliability. These devices are ideal for general purpose functions such as Gigabit Ethernet or dual PCI Express control planes, bridging functions, input/output (I/O) expansion and conversion, video/image processing, system management and secure connectivity. Microsemi FPGAs are used by customers in in Communications, Industrial, Medical, Defense, and Aviation markets.

- High-Performance Memory Subsystem
- PCIe Gen2 endpoints starting at 10 K Logic Elements

- Embedded DDR3 memory controllers
- SECDED memory protection
- 1 mW in Flash*Freeze mode

- Instant-on
- Zero FIT FPGA Configuration Cells
- CRI DPA Pass through license
- Small packages

- NRBG, AES-256, SHA-256, ECC Cryptographic Engine
- User Physically Unclonable Function (PUF)

IGLOO2 Devices

IGLOO2 Devices	Features	M2GL005	M2GL010	M2GL025	M2GL050	M2GL060	M2GL090	M2GL150
Logic/DSP	Maximum Logic Elements (4LUT + DFF)	6,060	12,084	27,696	56,340	56,520	86,184	146,124
	Mathblocks (18 x 18)	11	22	34	72	72	84	240
	PLLs and CCCs	2		6				8
	SPI/HPDMA/PDMA	1 each						
	Fabric Interface Controllers (FICs)	1			2	1		2
	Data Security	AES256, SHA256, RNG			AES256, SHA256, RNG, ECC, PUF			
Memory	eNVM (K Bytes)	128	256				512	
	LSRAM 18 K Blocks	10	21	31	69		109	236
	uSRAM 1 K Blocks	11	21	34	72		112	240
	eSRAM (K Bytes)	64						
	Total RAM (K bits)	703	912	1104	1826		2586	5000
High-Speed	DDR Controllers (count × width)	1×18			2×36	1×18		2x36
	SERDES Lanes	0	4		8	4		16
	PCIe End Points	0	1		2			4
User I/O	MSIO (3.3 V)	115	123	157	139	271	309	292
	MSIOD (2.5 V)	28	40		62	40		106
	DDRIO (2.5 V)	66	70		176	76		176
	Total User I/Os	209	233	267	377	387	425	574
Grades	Commercial (C), Industrial (I), Military (M)	C,I	C,I,M					

Notes:
1. Total logic may vary based on utilization of DSP and memories in your design. Please see the IGLOO2 and SmartFusion2 Fabric User Guide for details.
2. Feature availability is package dependent.

I/Os Per Package

Package Type	FCS(G)325		VF(G)256		FCS(G)536		VF(G)400		FCV(G)484		TQ(G)144		FG(G)484		FG(G)676		FG(G)896		FC(G)1152	
Package Options																				
Pitch (mm)	0.5		0.8		0.5		0.8				0.5		1.0		1.0		1.0		1.0	
Length x Width (mm)	11x11		14x14		16x16		17x17		19x19		20x20		23x23		27x27		31x31		35x35	
Device	I/O	Lanes	I/O	Lanes	I/O	Lanes	I/O	Lanes	I/O	Lanes	I/O	Lanes	I/O	Lanes	I/O	Lanes	I/O	Lanes	I/O	Lanes
M2GL005 (S)	—	—	161	—	—	—	171	—	—	—	84	—	209	—	—	—	—	—	—	—
M2GL010 (S/T/TS)	—	—	138	2	—	—	195	4	—	—	84	—	233	4	—	—	—	—	—	—
M2GL025 (T/TS)	180	2	138	2	—	—	207	4	—	—	—	—	267	4	—	—	—	—	—	—
M2GL050 (T/TS)	200	2	—	—	—	—	207	4	—	—	—	—	267	4	—	—	377	8	—	—
M2GL060 (T/TS)	200	2	—	—	—	—	207	4	—	—	—	—	267	4	387	4	—	—	—	—
M2GL090 (T/TS)	180	4	—	—	—	—	—	—	—	—	—	—	267	4	425	4	—	—	—	—
M2GL150 (T/TS)	—	—	—	—	293	4	—	—	248	4	—	—	—	—	—	—	—	—	574	16

Notes:
1. M2GL090 FCS325 package dimension is 11x13.5.   2. Highlighted devices can migrate vertically in the same package.   3. (G) indicates that the package is RoHS 6/6 Compliant/Pb-free.

IGLOO/e FPGA

The low-power programmable solution ideal for CPLD replacement

The IGLOO family of reprogrammable and full-featured flash FPGAs is designed to meet the low power and area requirements of today's portable electronics. Based on nonvolatile flash technology, the 1.2 V to 1.5 V operating voltage family offers the industry's low power consumption—as low as 5 µW. The IGLOO family supports up to 35 K logic elements with up to 504 Kbits of true dual-port SRAM, up to 6 embedded PLLs and up to 620 user I/Os. Low-power applications that require 32-bit processing can use the ARM Cortex-M1 processor without license fee or royalties in M1 IGLOO devices. Developed specifically for implementation in FPGAs, Cortex-M1 devices offer an optimal balance between performance and size to minimize power consumption.

- Low-power FPGAs
- Flash*Freeze technology for low power consumption
- 1.2 V core and I/O voltage
- Instant-on
- AES-protected in-system programming (ISP)
- User nonvolatile FlashROM

IGLOO/e Devices

IGLOO Devices	Features	AGL030	AGL060	AGL125	AGL250	AGL400	AGL600	AGL1000	AGLE600	AGLE3000
ARM-Enabled IGLOO Devices[1]					M1AGL250		M1AGL600	M1AGL1000		M1AGLE3000
Logic	Logic Elements (approximate)	330	700	1,500	3,000	5,000	7,000	11,000	7,000	35,000
	System Gates	30,000	60,000	125,000	250,000	400,000	600,000	1,000,000	600,000	3,000,000
	VersaNet Globals[3]	6	18	18	18	18	18	18	18	18
	Flash*Freeze Mode (typical, µW)	5	10	16	24	32	36	53	49	137
	AES-Protected ISP[1]	—	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes
	Integrated PLLs with CCC[2]	—	1	1	1	1	1	1	6	6
Fabric Memory	RAM (1,024 bits)	—	18	36	36	54	108	144	108	504
	RAM Blocks (4,608 bits)	—	4	8	8	12	24	32	24	112
	FlashROM K bits (1,024 bits)	1	1	1	1	1	1	1	1	1
User I/O	I/O Banks	2	2	2	4	4	4	4	8	8
	Maximum User I/Os	81	96	133	143	194	235	300	270	620

Notes:
1. AES is not available for Cortex-M1 IGLOO devices.
2. AGL060 in CS121 does not support the PLL.
3. Six chip (main) and twelve quadrant global networks are available for AGL060 devices and above.

I/Os Per Package

IGLOO/e Devices	I/O Package	QNG48	QNG68	UCG81	CSG81	CS(G)121	VQ(G)100	CS(G)196	FG(G)144	FG(G)256[3]	CS(G)281	FG(G)484[3]	FG(G)896
	Pitch (mm)	0.4	0.4	0.4	0.5	0.5	0.5	0.5	1.0	1.0	0.5	1.0	1.0
	Length x Width (mm)	6x6	8x8	4x4	5x5	6x6	16x16	8x8	13x13	17x17	10x10	23x23	31x31
AGL030	Single-End I/O	34	49	66	66	—	77	—	—	—	—	—	—
AGL060	Single-End I/O	—	—	—	—	96	71	—	—	—	—	—	—
AGL125	Single-End I/O	—	—	—	—	96	71	133	97	—	—	—	—
AGL250/ M1AGL250	Single-End I/O[2]	—	—	—	—	—	68	143[1]	97	—	—	—	—
	Differential I/O	—	—	—	—	—	13	35[1]	24	—	—	—	—
AGL400	Single-End I/O[2]	—	—	—	—	—	—	143	97	178	—	194	—
	Differential I/O	—	—	—	—	—	—	35	25	38	—	38	—
AGL600/ M1AGL600	Single-End I/O[2]	—	—	—	—	—	—	—	97	177	215	235	—
	Differential I/O	—	—	—	—	—	—	—	25	43	53	60	—
AGL1000/ M1AGL1000	Single-End I/O[2]	—	—	—	—	—	—	—	97	177	215	300	—
	Differential I/O	—	—	—	—	—	—	—	25	44	53	74	—
AGLE600	Single-End I/O[2]	—	—	—	—	—	—	—	—	165	—	270	—
	Differential I/O	—	—	—	—	—	—	—	—	79	—	135	—
AGLE3000/ M1AGLE3000	Single-End I/O[2]	—	—	—	—	—	—	—	—	—	—	341	620
	Differential I/O	—	—	—	—	—	—	—	—	—	—	168	310

Notes:
1. The M1AGL250 device does not support CS196 package.
2. Each used differential pair reduces the number of Single-End I/Os available by two.
3. FG256 and FG484 are footprint-compatible packages.

www.microsemi.com/products/fpga-soc/fpga/igloo-e

IGLOO nano FPGA

The industry's lowest power, smallest-size solution

IGLOO nano products offer ground breaking possibilities in power, size, lead-times, operating temperature and cost. Available in logic densities from 100 to 3 K logic elements, the 1.2 V to 1.5 V IGLOO nano devices have been designed for high-volume applications where power and size are key decision criteria. IGLOO nano devices are perfect ASIC or ASSP replacements, yet retain the historical FPGA advantages of flexibility and quick time-to-market in low power and small footprint profiles.

- Ultra low power in Flash*Freeze mode, as low as 2 µW
- Small footprint packages from 14×14 mm to 3×3 mm
- Enhanced commercial temperature
- 1.2 V to 1.5 V single voltage operation
- Enhanced I/O features
- Embedded SRAM and nonvolatile memory (NVM)
- ISP and security
- Instant-on

IGLOO nano Devices

IGLOO nano Devices	Features	AGLN010	AGLN020	AGLN060	AGLN125	AGLN250
Logic	Logic Elements (approximate)	100	200	700	1,500	3,000
	System Gates	10,000	20,000	60,000	125,000	250,000
	VersaNet Globals	4	4	18	18	18
	Flash*Freeze Mode (typical, µW)	2	4	10	16	24
	AES-Protected ISP	—	—	Yes	Yes	Yes
	Integrated PLL in CCCs[1]	—	—	1	1	1
Fabric Memory	RAM K bits (1,024 bits)	—	—	18	36	36
	4,608-bit Blocks	—	—	4	8	8
	FlashROM K bits (1,024 bits)	1	1	1	1	1
User I/O	I/O Banks	2	3	2	2	4
	Maximum User I/Os (packaged device)	34	52	71	71	68

Notes:
1. AGLN060, AGLN125 and AGLN250 in the CS(G)81 package do not support PLLs.

I/Os Per Package

I/O Packages	UCG36	QNG48	QNG68	UCG81	CSG81	VQ(G)100[2]
Pitch (mm)	0.4	0.4	0.4	0.4	0.5	0.5
Length x Width (mm)	3x3	6x6	8x8	4x4	5x5	16x16
AGLN010	23	34	—	—	—	—
AGLN020	—	—	49	52	52	—
AGLN060	—	—	—	—	60	71
AGLN125	—	—	—	—	60	71
AGLN250	—	—	—	—	60	68

Notes:
1. IGLOO nano devices do not support differential I/Os.
2. (G) indicates that the package is RoHS 6/6 Compliant/Pb-free.

IGLOO PLUS FPGA

The low-power FPGA with enhanced I/O capabilities

IGLOO PLUS products deliver low power and enhanced I/Os in a feature-rich programmable device, offering more I/Os per LE compared to the IGLOO devices and supports independent Schmitt trigger inputs, hot-swapping and Flash*Freeze bus hold. Ranging from 330 to 1.5 K logic elements, the 1.2 V to 1.5 V IGLOO PLUS devices have been optimized to meet the needs of I/O-intensive, power-conscious applications that require exceptional features.

- I/O-optimized FPGA
- Low power in Flash*Freeze mode, as low as 5 μW
- Small footprint and low-cost packages
- Reprogrammable flash technology
- 1.2 V to 1.5 V single voltage operation
- Embedded SRAM NVM
- AES-protected ISP
- Instant-on

IGLOO PLUS Devices

IGLOO PLUS Devices	Features	AGLP030	AGLP060	AGLP125
Logic	Logic Elements (approximate)	330	7,000	1,500
	System Gates	30,000	60,000	125,000
	VersaNet Globals	6	18	18
	Flash*Freeze Mode (typical, μW)	5	10	16
	AES-Protected ISP	—	Yes	Yes
	Integrated PLL in CCCs[1]	—	1	1
Fabric Memory	RAM (1,024 bits)	—	18	36
	4,608-bit Blocks	—	4	8
	FlashROM K bits (1,024 bits)	1	1	1
User I/O	I/O Banks	4	4	4
	Maximum User I/Os (packaged device)	120	157	212

Notes:
1. AGLP060 in CS(G)201 does not support the PLL.

I/Os Per Package

IGLOO PLUS Devices	I/O Package	CS(G)201	CS(G)281	CS(G)289	VQ(G)176
	Pitch (mm)	0.5	0.5	0.8	0.4
	Length x Width (mm)	8X8	10X10	14X14	22X22
AGLP030	Single-End I/O	120	—	120	—
AGLP060	Single-End I/O	157	—	157	137
AGLP125	Single-End I/O	—	212	212	—

Notes:
1. IGLOO Plus devices do not support differential I/Os.
2. (G) indicates that the package is RoHS 6/6 Compliant/Pb-free.

ProASIC3/E FPGA

Low density CPLD replacement FPGA

The ProASIC3 series of flash FPGAs offers a breakthrough in power, performance, density and features for today's most demanding high-volume applications. The ProASIC3 devices support the ARM Cortex-M1 processor, offering the benefits of programmability and time-to-market at low cost. The ProASIC3 devices are based on nonvolatile flash technology and support 330 to 35 K logic elements and up to 620 high-performance I/Os. For automotive applications, selected ProASIC3 devices are qualified to the AEC-Q100 and are available with AEC T1 screening and PPAP documentation.

- 1.5 V single voltage operation
- 350 MHz system performance
- Instant-on
- Configuration memory error immune
- Advanced I/O standards
- Secure ISP

ProASIC3/E Devices

ProASIC3/E Devices	Features	A3P030	A3P060[2]	A3P125[2]	A3P250[2]	A3P400	A3P600	A3P1000[2]	A3PE600	A3PE1500	A3PE3000
ARM Cortex-M1 Devices					M1A3P250	M1A3P400	M1A3P600	M1A3P1000		M1A3PE1500	M1A3PE3000
Logic	Logic Elements (approximate)	330	700	1,500	3,000	5,000	7,000	11,000	7,000	16,000	35,000
	System Gates	30,000	60,000	125,000	250,000	400,000	600,000	1,000,000	600,000	1,500,000	3,000,000
	VersaNet Globals[3]	6	18	18	18	18	18	18	18	18	18
	AES-Protected ISP[1]	—	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes
	Integrated PLL in CCCs	—	1	1	1	1	1	1	6	6	6
Fabric Memory	RAM (1,024 bits)	—	18	36	36	54	108	144	108	270	504
	4,608-bit Blocks	—	4	8	8	12	24	32	24	60	112
	FlashROM K bits (1,024 bits)	1	1	1	1	1	1	1	1	1	1
User I/O	I/O Banks	2	2	2	4	4	4	4	8	8	8
	Maximum User I/Os	81	96	133	157	194	235	300	270	444	620

Notes:
1. AES is not available for Cortex-M1 ProASIC3 devices.
2. Available as automotive "T" grade
3. Six chip (main) and three quadrant global networks are available for A3P060 and above.

I/Os Per Package

ProASIC3	I/O Type	QNG48	QNG68	CS(G)121	VQ(G)100	TQ(G)144	PQ(G)208	FG(G)144	FG(G)256	FG(G)324	FG(G)484	FG(G)676	FG(G)896
	Pitch (mm)	0.4	0.4	0.5	0.5	0.5	0.5	1.0	1.0	1.0	1.0	1.0	1.0
	Length x Width (mm)	6x6	8x8	6x6	16x16	20x20	30.6x30.6	13x13	17x17	19x19	23x23	27x27	31x31
A3P030	Single-End I/O	34	49	—	77	—	—	—	—	—	—	—	—
A3P060	Single-End I/O	—	—	96	71	91	—	96	—	—	—	—	—
A3P125	Single-End I/O	—	—	—	71	100	133	97	—	—	—	—	—
A3P250/ M1A3P250	Single-End I/O	—	—	—	68	—	151	97	157	—	—	—	—
	Differential I/O	—	—	—	13	—	34	24	38	—	—	—	—
A3P400/ M1A3P400	Single-End I/O	—	—	—	—	—	151	97	178	—	194	—	—
	Differential I/O	—	—	—	—	—	34	25	38	—	38	—	—
A3P600/ M1A3P600	Single-End I/O	—	—	—	—	—	154	97	177	—	235	—	—
	Differential I/O	—	—	—	—	—	35	25	43	—	60	—	—
A3P1000/ M1A3P1000	Single-End I/O	—	—	—	—	—	154	97	177	—	300	—	—
	Differential I/O	—	—	—	—	—	35	25	44	—	74	—	—
A3PE600	Single-End I/O	—	—	—	—	—	147	—	165	—	270	—	—
	Differential I/O	—	—	—	—	—	65	—	79	—	135	—	—
A3PE1500/ M1A3PE1500	Single-End I/O	—	—	—	—	—	147	—	—	—	280	444	—
	Differential I/O	—	—	—	—	—	65	—	—	—	139	222	—
A3PE3000/ M1A3PE3000	Single-End I/O	—	—	—	—	—	147	—	—	221	341	—	620
	Differential I/O	—	—	—	—	—	65	—	—	110	168	—	310

Notes:
1. (G) indicates that the package is RoHS 6/6 Compliant/Pb-free.

ProASIC3 nano FPGA

Low density CPLD replacement FPGA with small package footprint

Microsemi's innovative ProASIC3 nano devices bring a new level of value and flexibility to high-volume markets. When measured against the typical project metrics of performance, cost, flexibility and time-to-market, the ProASIC3 nano devices provide an attractive alternative to ASICs and ASSPs in fast moving or highly competitive markets. Customer-driven total system cost reduction was a key design criteria for the ProASIC3 nano program. A single-chip implementation and a broad selection of small footprint packages, all contribute to lower total system costs.

- 1.5 V core for low power
- 350 MHz system performance
- Configuration memory error immune
- Enhanced commercial temperature
- Enhanced I/O features
- ISP and security

ProASIC3 nano Devices

ProASIC3 nano Devices	Features	A3PN010	A3PN020	A3PN060	A3PN125	A3PN250
Logic	Logic Elements (approximate)	100	200	700	1,500	3,000
	System Gates	10,000	20,000	60,000	125,000	250,000
	VersaNet Globals	4	4	18	18	18
	AES-Protected ISP	—	—	Yes	Yes	Yes
	Integrated PLL in CCCs	—	—	1	1	1
Fabric Memory	RAM (1,024 bits)	—	—	18	36	36
	4,608-bit Blocks	—	—	4	8	8
	FlashROM Kbits (1,024 bits)	1	1	1	1	1
User I/O	I/O Banks	2	3	2	2	4
	Maximum User I/Os (packaged device)	34	49	71	71	68

I/Os Per Package

I/O Packages	QNG48	QNG68	VQ(G)100[1]
Pitch (mm)	0.4	0.4	0.5
Length x Width (mm)	6x6	8x8	16x16
A3PN010	34	—	—
A3PN020	—	49	—
A3PN060	—	—	71
A3PN125	—	—	71
A3PN250	—	—	68

Notes:
1. (G) indicates that the package is RoHS 6/6 Compliant/Pb-free.
2. ProASIC3 nano devices do not support differential I/Os.

ProASIC3L FPGA

Low density CPLD replacement FPGA with low power

ProASIC3L FPGAs feature lower dynamic power and lower static power than the previous generation ProASIC3 FPGAs and orders of magnitude lower power than SRAM competitors, combining dramatically reduced power consumption with up to 350 MHz operation. The ProASIC3L family also supports the free implementation of an FPGA-optimized 32-bit ARM Cortex-M1 processor, enabling system designers to select Microsemi's flash FPGA solution that best meets their speed and power design requirements, regardless of application or volume. Optimized software tools using power-driven layout (PDL) provide instant power reduction capabilities.

- Low power 1.2 V to 1.5 V core operation
- 700 Mbps DDR, LVDS capable I/Os
- Up to 350 MHz system performance
- Configuration memory error immune
- ISP and security
- Flash*Freeze technology for low power

ProASIC3L Low-Power Devices

ProASIC3L Devices	Features	A3P250L	A3P600L	A3P1000L	A3PE3000L
ARM Cortex-M1 Devices[1]			M1A3P600L	M1A3P1000L	M1A3PE3000L
Logic	Logic Elements (approximate)	3,000	7,000	11,000	35,000
	System Gates	250,000	600,000	1,000,000	3,000,000
	VersaNet Globals	18	18	18	18
	AES-Protected ISP[2]	Yes	Yes	Yes	Yes
	Integrated PLL in CCCs[3]	1	1	1	6
Fabric Memory	RAM (1,024 bits)	36	108	144	504
	4,608-bit Blocks	8	24	32	112
	FlashROM K bits (1,024 bits)	1	1	1	1
User I/O	I/O Banks	4	4	4	8
	Maximum User I/Os (packaged device)	157	235	300	620

Notes:
1. Refer to the Cortex-M1 product brief for more information.
2. AES is not available for Cortex-M1 ProASIC3L devices.
3. For the A3PE3000L, the PQ208 package has six CCCs and two PLLs.

I/Os Per Package

ProASIC3L Devices	I/O Type	VQ(G)100	PQ(G)208	FG(G)144	FG(G)256	FG(G)324	FG(G)484	FG(G)896
	Pitch (mm)	0.5	0.5	1.0	1.0	1.0	1.0	1.0
	Length x Width (mm)	16x16	30.6x30.6	13x13	17x17	19x19	23x23	31x31
A3P250L	Single-End I/O	68	151	97	157	—	—	—
	Differential I/O	13	34	24	38	—	—	—
A3P600L/ M1A3P600L	Single-End I/O	—	154	97	177	—	235	—
	Differential I/O	—	35	25	43	—	60	—
A3P1000L/ M1A3P1000L	Single-End I/O	—	154	97	177	—	300	—
	Differential I/O	—	35	25	44	—	74	—
A3PE3000L/ M1A3PE3000L	Single-End I/O	—	147	—	—	221	341	620
	Differential I/O	—	65	—	—	110	168	310

Notes:
1. (G) indicates that the package is RoHS 6/6 Compliant/Pb-free.

SmartFusion SoC FPGA

SmartFusion SoCs integrates an FPGA fabric, an ARM Cortex-M3 processor and a programmable analog, offering full customization, IP protection and ease-of-use. Based on Microsemi's proprietary flash process, SmartFusion cSoCs are ideal for hardware and embedded designers who need a true system-on-chip that gives more flexibility than traditional fixed-function microcontrollers without the excessive cost of soft processor cores on traditional FPGAs.

- Available in commercial, industrial and military grades
- Hard 100 MHz 32-bit ARM Cortex-M3 CPU
- Multi-layer AHB communications matrix with up to 16 Gbps throughput

- 10/100 Ethernet MAC
- Two peripherals of each type: SPI, I2C, UART and 32-bit timers
- Up to 512 KB flash and 64 KB SRAM
- External memory controller (EMC)

- 8-channel DMA controller
- Integrated analog-to-digital converters (ADCs) and digital-to-analog converters (DACs) with 1 percent accuracy
- On-chip voltage, current and temperature monitors

- Up to ten 15 ns high-speed comparators
- Analog compute engine (ACE) offloads CPU from analog processing
- Up to 35 analog I/Os and 169 digital GPIOs

SmartFusion Devices

SmartFusion Devices	Features	A2F060	A2F200	A2F500
Logic	Logic Elements (approximate)	700	2,000	6,000
	System Gates	60,000	200,000	500,000
	RAM Blocks (4,608 bits)	8	8	24
Microcontroller Subsystem (MSS)	Flash (K bytes)	128	256	512
	SRAM (K bytes)	16	64	64
	Cortex-M3 with Memory Protection Unit (MPU)	Yes	Yes	Yes
	10/100 Ethernet MAC	No	Yes	Yes
	External Memory Controller (EMC)	26-bit address, 16-bit data[1]	26-bit address, 16-bit data	26-bit address, 16-bit data[1]
	DMA	8 Ch	8 Ch	8 Ch
	I2C	2	2	2
	SPI	2	2	2
	16550 UART	2	2	2
	32-bit Timer	2	2	2
	PLL	1	1	2[2]
	32 kHz Low Power Oscillator	1	1	1
	100 MHz On-Chip RC Oscillator	1	1	1
	Main Oscillator (32 KHz to 20 MHz)	1	1	1
Programmable Analog	ADCs (8-/10-/12-bit SAR)	1	2	3[4]
	DACs (12-bit sigma-delta)	1	2	3[4]
	Signal Conditioning Blocks (SCBs)	1	4	5[4]
	Comparators[3]	2	8	10[4]
	Current Monitors[3]	1	4	5[4]
	Temperature Monitors[3]	1	4	5[4]
	Bipolar High Voltage Monitors[3]	2	8	10[4]

Notes:
1. Not available on A2F500 for the PQ208 package and A2F060 for the TQ144 package.
2. Two PLLs are available in CS288 and FG484, one PLL in FG256 and PQ208.
3. These functions share I/O pins and may not all be available at the same time. See the "Analog Front-End Overview" section in the SmartFusion Programmable Analog User's Guide for details.
4. Available on FG484 only. PQ208, FG256 and CS288 packages offer the same programmable analog capabilities as A2F200.

Package I/Os: MSS + FPGA I/Os

Device	A2F060[1]			A2F200[2]				A2F500[2]			
	TQ(G)144	CS(G)288	FG(G)256	PQ(G)208	CS(G)288	FG(G)256	FG(G)484	PQ(G)208	CS(G)288	FG(G)256	FG(G)484
Pitch (mm)	0.5	0.5	1.0	0.5	0.5	1.0	1.0	0.5	0.5	1.0	1.0
Length x Width (mm)	20x20	11x11	17x17	30.6x30.6	11x11	17x17	23x23	30.6x30.6	11x11	17x17	23x23
Direct Analog Inputs	11	11	11	8	8	8	8	8	8	8	12
Shared Analog Inputs[1]	4	4	4	16	16	16	16	16	16	16	20
Total Analog Input	15	15	15	24	24	24	24	24	24	24	32
Total Analog Output	1	1	1	1	2	2	2	1	2	2	3
MSS I/Os[5]	21[4]	28[4]	26[4]	22	31	25	41	22	31	25	41
FPGA I/Os	33[3]	68	66	66	78	66	94	66[3]	78	66	128
Total I/Os	70	112	108	113	135	117	161	113	135	117	204

Notes:
1. There are no LVTTL capable direct inputs available on A2F060 devices.
2. These pins are shared between direct analog inputs to the ADCs and voltage/current/temperature monitors.
3. EMC is not available on the A2F500 PQ208 and A2F060 TQ144 package.
4. 10/100 Ethernet MAC is not available for A2F060.
5. 16 MSS I/Os are multiplexed and can be used as FPGA I/Os, if not required for MSS. These I/Os support Schmitt triggers, and support only LVTTL and LVCMOS (1.5 V / 1.8 V / 2.5 V / 3.3 V) standards.
6. (G) indicates that the package is RoHS 6/6 Compliant/Pb-free.

Military SmartFusion2, IGLOO2

FPGAs for military applications

Microsemi is the leader in serving high reliability defense applications for over 25 years. Microsemi FPGAs are qualified to Mil Std 883 Class B and QML class Q. Based on flash architecture, Microsemi offers industry's most reliable and low-power FPGAs and SoC FPGAs. Military grade FPGAs are available in IGLOO2, ProASICPlus and ProASIC3/EL device families and SoC FPGAs are available in SmartFusion2, SmartFusion and Fusion device families. In addition to the advantages of the mainstream FPGAs, SoC FPGAs have an Embedded ARM Cortex-M3 microcontroller on-chip. SmartFusion and Fusion devices integrate configurable analog peripherals to yield a true system-on-chip solution.

- Tested for temperature range of -55ºC to +125ºC for high reliability
- Product longevity
- ISO-9001 and AS-9100 certified quality management system

- PCI Express Gen1 endpoints
- Instant-on
- Small packages
- Zero FIT FPGA Configuration Cells

- SECDED memory protection
- Built-in tamper detection and zeroization capability
- NRBG, AES-256, SHA-256, ECC Cryptographic Engine

- User Physically Unclonable Function (PUF)
- CRI DPA Pass through license
- Lowest power operation
- Embedded ARM Cortex-M3 Microcontroller Subsystem

Military SmartFusion2 and IGLOO2 Devices

SmartFusion2/ IGLOO2	Features	M2GL010 M2S010	M2GL025 M2S025	M2GL050 M2S050	M2GL060 M2S060	M2GL090 M2S090	M2GL150 M2S150
Logic/DSP	Maximum Logic Elements (4LUT+DFF)	12,084	27,696	56,340	56,520	86,184	146,124
	Mathblocks (18 x 18)	22	34	72	72	84	240
	PLLs and CCCs	2	6				8
	MSS (SmartFusion2) or HPMS (IGLOO2)	1					
	Security	AES256, SHA256, RNG			AES256, SHA256, RNG, ECC, PUF		
Memory	eNVM (K Bytes)	256				512	
	eSRAM (K Bytes)	64					
	LSRAM 18 K Blocks	21	31	69	69	109	236
	uSRAM 1 K Blocks	22	34	72	72	112	240
	Total Fabric RAM (K bits)	400	592	1314	1314	2074	4488
	Total RAM (K bits)	912	1104	1826	1826	2586	5000
High-Speed	DDR Controllers	1x18					2x36
	SERDES Lanes	4					16
	PCIe End Points	1			2		4
User I/O	MSIO (3.3 V)	123	157	105	157	157	292
	MSIOD (2.5 V)	40	40	40	40	40	106
	DDRIO (2.5 V)	70	70	122	70	70	176
	Total User I/O	233	267	267	267	267	574
Package		FG(G)484M	FG(G)484M	FG(G)484M	FG(G)484M	FG(G)484M	FC(G)1152M

I/Os Per Package

Package Type	Package Options			
	FG(G)484		FC(G)1152	
Pitch (mm)	1.0		1.0	
Length x Width (mm)	23x23		35x35	
Device	I/O	Lanes	I/O	Lanes
M2S010 / M2GL010 (T/TS)	233	4	—	—
M2S025 / M2GL025 (T/TS)	267	4	—	—
M2S050 / M2GL050 (T/TS)	267	4	—	—
M2S060 / M2GL060 (T/TS)	267	4	—	—
M2S090 / M2GL090 (T/TS)	267	4	—	—
M2S150 / M2GL150 (T/TS)	—	—	574	16

Notes:
1. Can migrate vertically in the same package.
2. Gold wire bonds are available for the FG484 package by appending X399 to the part number when ordering, for example: M2S090 (T/TS)-1FG484MX399.
3. All the packages are available with lead and lead free. (G) indicates that the package is RoHS 6/6 Compliant/Pb-free.

Military SmartFusion, ProASIC3 and Fusion

Military SmartFusion, ProASIC3 and Fusion Devices

Devices	Features	A3P250	A3PE600L	A3P1000	A3PE3000L	AFS600	AFS1500	A2F060	A2F500
ARM Cortex-M1 Devices[1]				M1A3P1000	M1A3PE3000L	M1AFS600	M1AFS1500	Hard 32-bit ARM Cortex-M3	Hard 32-bit ARM Cortex-M3
Logic	Logic Elements (approximate)	3,000	7,000	11,000	35,000	7,000	16,000	700	6,000
	System Gates	250,000	600,000	1,000,000	3,000,000	600,000	1,500,000	60,000	500,000
	PLL	1	6	1	6	2	2	1	2
	ADCs (8-,10-,12-bit SAR)	—	—	—	—	1	1	1	3
	AES-Protected ISP[1]	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes
Fabric memory	RAM (1,024 bits)	36	108	144	504	108	270	16	64
	RAM Blocks (4,608 bits)	8	24	32	112	24	60	8	24
User I/O	Maximum User I/Os	68	270	300	620	212	263	108	204
	Digital I/Os	68	270	300	620	172	223	92	169
	Analog I/Os	—	—	—	—	40	40	16	35

Notes:
1. Refer to ARM Cortex-M1 Product Brief for more information.
2. AES is not available for ARM-enabled devices.

I/Os Per Package

Devices	I/O Type	VQ(G)100	PQ(G)208	FG(G)144	FG(G)256	FG(G)484	FG(G)896
	Pitch (mm)	0.5	0.5	1.0	1.0	1.0	1.0
	Length x Width (mm)	16x16	30.6x30.6	13x13	17x17	23x23	31x31
A3P250	Single-End I/O	68	—	—	—	—	—
	Differential I/O	13	—	—	—	—	—
A3PE600L	Single-End I/O	—	—	—	—	270	—
	Differential I/O	—	—	—	—	135	—
A3P1000/M1A3P1000	Single-End I/O	—	154	97	177	300	—
	Differential I/O	—	35	25	44	74	—
A3PE3000L/M1A3PE3000L	Single-End I/O	—	—	—	—	341	620
	Differential I/O	—	—	—	—	168	310
AFS600	Single-End I/O	—	—	—	119	172	—
	Differential I/O	—	—	—	58	86	—
AFS1500	Single-End I/O	—	—	—	119	223	—
	Differential I/O	—	—	—	58	109	—
A2F060	Analog I/O	—	—	—	16	—	—
	FPGA I/O	—	—	—	66	—	—
	MSS I/O	—	—	—	26	—	—
A2F500	Analog I/O	—	—	—	26	35	—
	FPGA I/O	—	—	—	66	128	—
	MSS I/O	—	—	—	25	41	—

Notes:
1. (G) indicates that the package is RoHS 6/6 Compliant/Pb-free.

Automotive Grade Products

Microsemi offers dedicated automotive grade devices in various densities, features, footprints and temperature grades. All devices and packages are AEC-Q100 qualified and tested at extended temperatures. PPAP documentation is available for ProASIC3 devices on request.

SmartFusion2 SoC FPGA Product Family

	Features	M2S005S	M2S010TS	M2S025TS	M2S060TS	M2S090TS
Logic/DSP	Maximum Logic Elements (4LUT + DFF)[1]	6,060	12,084	27,696	56,520	86,184
	Math Blocks (18x18)	11	22	34	72	84
	Fabric Interface Controllers (FICs)	1				
	PLLs and CCCs	2		6		
	Data Security	AES256, SHA256, RNG			AES256, SHA256, RNG, ECC, PUF	
MSS	Cortex-M3 + Instruction cache	Yes				
	eNVM (K Bytes)	128	256		512	
	eSRAM (K Bytes)	64				
	eSRAM (K Bytes) Non SECDED	80				
	CAN, 10/100/1000 Ethernet, HS USB	1 each				
	Multi-Mode UART, SPI, I2C, Timer	1 each				
High-Speed	DDR Controllers (Count x Width)	1 × 18				
	SERDES Lanes (T)	0	4			
	PCIe End Points	0	1		2	
User I/Os	MSIO (3.3 V)	115	123	157	271	309
	MSIOD (2.5 V)	28	40	40	40	40
	DDRIO (2.5 V)	66	70	70	76	76
	TOTAL USER I/O	209	233	267	387	425

Notes :

1. Total logic may vary based on utilization of DSP and memories in the design.

2. Feature availability is package dependent.

Package Options

Type	VFG256[1]		VFG400[1]		FGG484[1]		FGG676[1]	
Pitch (mm)	0.8		0.8		1		1	
Length × Width (mm)	14 × 14		17 × 17		23 × 23		27 × 27	
Device	I/O	Lanes	I/O	Lanes	I/O	Lanes	I/O	Lanes
M2S005S	161	-	171	-	209	-	–	–
M2S010TS	138	2	195	4	233	4	–	–
M2S025TS	138	2	207	4	267	4	–	–
M2S060TS	–	–	207	4	267	4	387	4
M2S090TS	–	–	–	–	267	4	425	4

Note :

1. All Automotive packages are RoHS compliant and available in lead free options only.

2. Shade indicates that device packages have vertical migration capability.

Automotive Grade Products

IGLOO2 FPGA Product Family

	Features	M2GL005S	M2GL010TS	M2GL025TS	M2GL060TS	M2GL090TS
Logic/DSP	Maximum Logic Elements (4LUT + DFF)[1]	6,060	12,084	27,696	56,520	86,184
	Math Blocks (18x18)	11	22	34	72	84
	PLLs and CCCs	2		6		
	SPI/HPDMA/PDMA	1 each				
	Fabric Interface Controllers (FICs)	1				
	Data Security	AES256, SHA256, RNG			AES256, SHA256, RNG, ECC, PUF	
Memory	eNVM (K Bytes)	128	256			512
	LSRAM 18 K Blocks	10	21	31	69	109
	uSRAM1 K Blocks	11	22	34	72	112
	eSRAM (K Bytes)	64				
	Total RAM (K bits)	703	912	1104	1826	2586
High Speed	DDR Controllers (Count x Width)	1×18				
	SERDES Lanes (T)	0	4			
	PCIe End Points	0	1		2	
User I/Os	MSIO (3.3 V)	115	123	157	271	309
	MSIOD (2.5 V)	28	40	40	40	40
	DDRIO (2.5 V)	66	70	70	76	76
	Total User I/O	209	233	267	387	425

Note :

1. Total logic may vary based on utilization of DSP and memories in the design.

2. Feature availability is package dependent.

Package Options

Type	VFG256[1]		VFG400[1]		FGG484[1]		FGG676[1]	
Pitch (mm)	0.8		0.8		1		1	
Length x Width (mm)	14 × 14		17 × 17		23 × 23		27 × 27	
Device	I/O	Lanes	I/O	Lanes	I/O	Lanes	I/O	Lanes
M2S005S	161	-	171	-	209	–	–	–
M2S010TS	138	2	195	4	233	4	–	–
M2S025TS	138	2	207	4	267	4	–	–
M2S060TS	–	–	207	4	267	4	387	4
M2S090TS	–	–	–	–	267	4	425	4

Note :

1. All Automotive packages are RoHS compliant and available in lead free options only.

2. Shade indicates that device packages have vertical migration capability.

Automotive Grade Products

The table below serves as a guide to choose the right device for your applications. In addition, Microsemi offers more detailed product tables, Product Briefs, and Datasheets to assist in device selection.

Family	Logic Elements	Temperature Range	Max User I/Os	Max SERDES
IGLOO2[1]	6K to 86K	Grade 1 (-40°C to +135°C) Grade 2 (-40°C to +125°C)	Up to 425	4[1]
SmartFusion2	6K to 86K	Grade 2 (-40°C to +125°C)	Up to 425	4
ProASIC3	330 to 11K	Grade 1 (-40°C to +135°C) Grade 2 (-40°C to +115°C)	Up to 300	Not Available

Note. 1. SERDES is only supported in the IGLOO2 devices for the Grade 2 temperature range and not on Grade 1 temperature range.

ProASIC3 FPGA Product Family

	Features	A3P060	A3P125	A3P250	A3P1000
Logic	System Gates	60,000	125,000	250,000	1,000,000
	Equivalent LEs	700	1,500	3,000	11,000
	VersaNet Globals	18	18	18	18
	AES-Protected ISP[1]	Yes	Yes	Yes	Yes
	Integrated PLL in CCCs	1	1	1	1
Fabric Memory	RAM (1,024 bits)	18	36	36	144
	4,608-Bit Blocks	4	8	8	32
	FlashROM K bits (1,024 bits)	1	1	1	1
User I/O	I/O Banks	2	2	4	4
	Maximum User I/Os	96	133	157	300
Speed Grade	Speed Grades	Std.,-1	Std.,-1	Std.,-1	Std.,-1

Note :

1. Six chip (main) and three quadrant global networks are available for A3P060 and above

Package Options

Features	A3P060	A3P125	A3P250	A3P1000
Pitch (mm)	0.5	1	1	1
Length × Width (mm)	16 × 16	13 × 13	17 × 17	23 × 23
Device	I/O	I/O	I/O	I/O
A3P060	71	96	–	–
A3P125	71	97	–	–
A3P250	68/13	97/24	157/38	–
A3P1000	–	97/25	177/44	300/74

Ecosystem for Microsemi FPGAs and Soc FPGAs
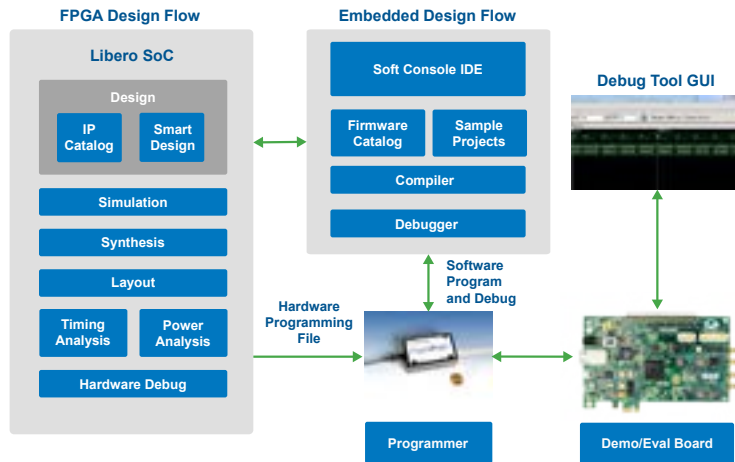
Libero® SoC and Libero® IDE

Libero System-on-Chip (SoC) and Libero Integrated Design Environment (IDE) are comprehensive software toolsets for designing with Microsemi FPGAs. Different versions of Libero support different families (see Licensing Requirements table for more details).

- Libero IDE software supports designing with the older Microsemi Rad-Tolerant FPGAs, Antifuse FPGAs and Legacy Flash FPGAs and managing the entire design flow from design entry, synthesis and simulation, through place-and-route, timing and power analysis.

- Libero SoC supports Microsemi's IGLOO2, SmartFusion2, SmartFusion, IGLOO, ProASIC3 and Fusion families managing the entire design flow from design entry, synthesis and simulation, through place-and-route, timing and power analysis, with enhanced integration of the embedded design flow. Libero SoC also includes a new System Builder design approach for correct by construction SoC FPGA configuration.

Standalone tools such as Silicon Sculptor, FlashPro and Synphony Model Compiler AE are not changing and will continue to include support for all silicon devices.Two types of Libero licenses are available. Libero Gold Free licenses cover the majority of mainstream FPGAs, while Libero Platinum supports the high end and advanced feature devices.

Licensing Requirements

Product Family	Device	License	
		Gold (FREE)	Platinum/Standalone
SmartFusion2/IGLOO2	M2S005, M2S010, M2S025, M2S050, M2S060, M2GL005, M2GL010, M2GL025, M2GL050, M2GL060, M2S005S[1], M2S010S[1], M2GL005S[1], M2GL010[1]	✓	✓
	M2S090, M2S150, M2GL090, M2GL150 All TS (Security) devices require a Platinum License.	NA	✓
SmartFusion, IGLOO, ProASIC3, Fusion and ProASIC PLUS	All Devices	✓	✓

Notes:
1. Available for free from Libero SoC v11.6.

Licensing Features

License Features	Libero Gold[1]	Libero Platinum[1]	Libero Standalone
License Term	1 Year	1 Year	1 Year
Libero Design Software, including SmartDesign, IP Catalog and Place and Route	✓	✓	✓
SoftConsole[2]	✓	✓	✓
FlashPro Software	✓	✓	✓
Synopsys Synplify Pro AE, ModelSim AE, Synopsys Identify AE	✓	✓	Not Included
Price	$ 0	$ 2,495	$ 995

Notes:
1. Gold and Platinum licenses have support for same IP Cores.
2. The following software is not supported on the Linux platforms: SoftConsole and Firmware Catalog.

www.microsemi.com/fpga-soc/design-resources/design-software/libero-soc

Ecosystem for Microsemi FPGAs and Soc FPGAs

Libero System Builder

Libero System Builder makes it easy to configure various subsystems and generate required Application Programming Interface (API) that implements a correct-by-construction infrastructure for your application. It can be used to configure the SmartFusion2 MSS block (peripherals and memory),FPGA fabric, peripherals and memory based on high level design specifications.

Libero SoftConsole

Libero SoftConsole provides a flexible, easy-to-use GUI for managing embedded software development projects. SoftConsole enables users to quickly develop, edit and debug software programs.

IAR Embedded Workbench

IAR Embedded Workbench is the Integrated development environment(IDE) from IAR Systems for building and debugging embedded applications of SmartFusion2 and SmartFusion. It includes project manager, editor, build and debugger tools.

Keil Microcontroller Development Kit (MDK)

Keil Microcontroller Development Kit (MDK) provides an easy compiling and debugging tools library for embedded applications using MSS block of SmartFusion2 and SmartFusion.

Embedded Design Support

Software IDE	SoftConsole	Keil MDK	IAR Embedded Workbench®
Free Versions from Microsemi	Free with Libero SoC	32 K Code Limited	32 K Code Limited
Available from Vendor	N/A	Full version	Full Version
Compiler	GNU GCC	RealView® C/C++	IAR ARM Compiler
Debugger	GDB Debug	µVision Debugger	C-SPY® Debugger
Instruction Set Simulator	No	µVision Simulator	Yes
Debug Hardware	FlashPro4/5	ULINK®2 or ULINK-ME	J-LINK™ or J-LINK Lite
Trace Capability	No	ULINKpro	JTAGjet-Trace

Go to www.microsemi.com/fpga-soc/design-resources/design-software/libero-soc for system requirements.

Debug

Microsemi's design debug tools and features compliment design simulations and development by allowing verification and troubleshooting at the hardware level. Having successfully passed functional and post-layout simulations, Microsemi's design debug tools can help provide the designer with a pre-system level implementation early warning of other design issues. Microsemi design debug focuses on analysis of the key elements of a flash design such as the embedded non-volatile memory (eNVM) data, SRAM data, Logic Elements, and System Builder blocks.

Microsemi's debug software is available in two variants:

SmartDebug

A Microsemi proprietary tool that allows the FPGA designers to quickly find and correct functional design bugs by probing the internal static and dynamic signals, eNVM and u/LSRAM Memory block and SERDES block of the FPGA. This tool supports IGLOO2 and SmatFusion2 only.

Identify ME®

Identify ME is a 3rd party On-chip debugging tool from Synopsys that allows the Microsemi FPGA designer to quickly find and correct functional design bugs by probing internal signals of the design directly from the flash FPGA at the system speed.

Identify ME SmartDebug Flow

Design Creation

Identify Instrumentation

Synthesis

Place and Route

Programming

Flash Device Programming ↔ Identify ME / SmartDebug

Microsemi Device
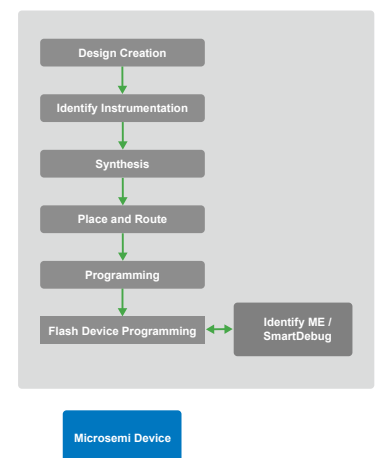
Development Kits

SmartFusion2 Starter Kit
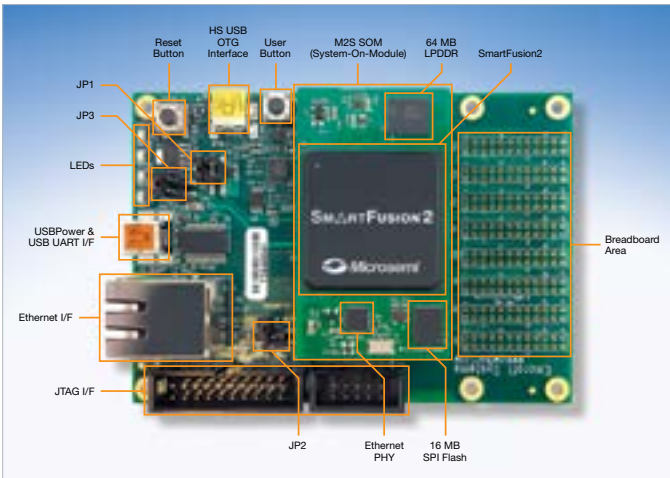
- Cost-efficient development platform for SmartFusion2 SoC FPGA
- Supports industry-standard interfaces including Ethernet, USB, SPI, I2C and UART
- Preloaded with uClinux image to support Linux-based development environments
- Comes with FlashPro4 programmer, USB cables and USB WiFi module

- Board features
  - 50 K LE or 10 K LE SmartFusion2 device
  - JTAG interface for programming and debug
  - 10/100 Ethernet
  - USB 2.0 On-The-Go
  - 64 MB LPDDR, 16 MB SPI Flash memory
  - 4 LEDs and 2 push-button switches
  - On-module clocks
  - Watchdog timer (WDT)

Ordering Code	Supported Device	Price
SF2-STARTER-KIT	M2S050-FGG484	$ 299
SF2-484-STARTER-KIT	M2S010-FGG484	$ 299

SmartFusion2 Advanced Development Kit
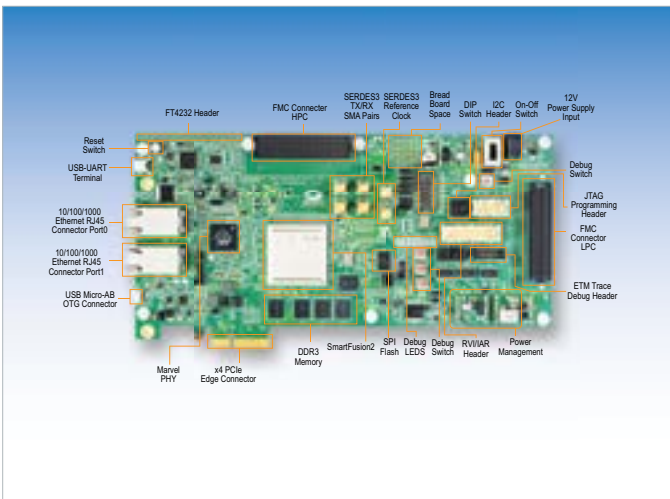
- Full featured kit to develop applications using SmartFusion2 SoC FPGAs
- Enables power measurement
- Two FMC connectors with HPC/LPC pinout for expansion
- Various communication interfaces, switches and LEDs for prototyping
- Kit comes with free 1-year platinum Libero SoC license
- Board features
  - 150 K LE SmartFusion2 device
  - DDR3 SDRAM, SPI flash
  - Current measurement test points

- A pair of SMA connectors, two FMC connectors, PCIe x4 edge connector
- 2xRJ45 interface for 10/100/1000 Ethernet USB micro-AB connector
- FTDI programmer interface to program the external SPI flash
- JTAG/SPI programming interface, RVI header for application programming and debug
- Quad 2:1 MUX/DEMUX high bandwidth bus switch
- Dual in-line package (DIP) switches for user application
- Push-button switches and LEDs for demo purposes

Ordering Code	Supported Device	Price
M2S150-ADV-DEV-KIT	M2S150TS-1FCG1152	$ 999

SmartFusion2 Security Evaluation Kit
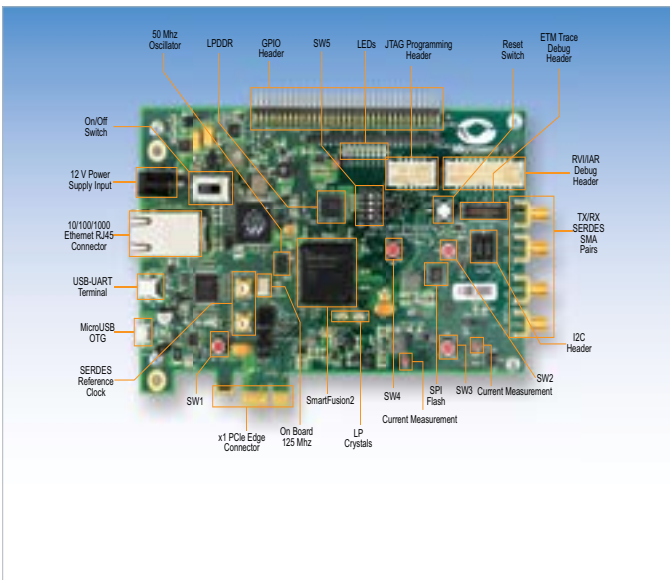
- Evaluate the Data Security features of SmartFusion2 SoC FPGAs
- Develop and test PCI Express Gen2 x1 lane designs
- Test the signal quality of the FPGA transceiver using full-duplex SERDES SMA Pairs
- Measure the low power consumption of the SmartFusion2 SoC FPGA
- Quickly create a working PCIe link with the included PCIe Control Plane Demo
- Kit includes free 1-year platinum Libero SoC license

- Board features
  - 90 K LE SmartFusion2 device
  - 64 Mb SPI Flash memory
  - 512 MB LPDDR
  - PCI Express Gen2 x1 interface
  - Four SMA connector for testing of full-duplex SERDES channel
  - RJ45 interface for 10/100/1000 Ethernet
  - JTAG/SPI programming interface
  - Headers for I2C, SPI, GPIOs
  - Push-button switches and LEDs for demo purposes
  - Current Measurement Test Points

Ordering Code	Supported Device	Price
M2S090TS-EVAL-KIT	M2S090TS-FGG484	$ 399

Development Kits

Avnet SmartFusion2 KickStart Kit

SmartFusion2 KickStart Kit includes

- SmartFusion2 SoC M2S010TQ144
- Bluetooth 4.1 Low Energy Module
- Quad Channel Power Manager
- Power-On-Reset
- Ambient Light Sensor
- Motion and Temperature Sensor
- 4 User LEDs
- 50 MHz Oscillator Module
- 2kbit Serial EEPROM for FTDI Chip
- 3x 12-Pin PMOD-Compatible Connectors
- Arduino Carrier Card Support

Avnet's SmartFusion2 KickStart Kit includes HDL and C-Code reference design files that demonstrate all of the key architectural features of the SmartFusion2 device. These design files are ideal for an engineer to modify to start their own designs.

- Example connects all the on-board peripherals and includes a windows GUI that allows complete communication with the SmartFusion2, perfect as a template for a users design.

- Data Security reference design demonstrates how a secure communications link is established between a SmartFusion2 device and an Android phone/tablet over Bluetooth Low Energy.

Ordering Code	Supported Device	Price
AES-SF2-KSB-G	M2S010-TQ144	$59.95 available from Avnet

Arrow SF2+ Development Kitt

The SF2+ Development Kit Includes

- M2S010 SOM with LPDDR, SPI Flash, Ethernet PHY (Additional Emcraft SmartFusion2 SOMs available)
- Timberwolf Audio Processor with 2 MEMs MICs and Speaker Jack
- Microsemi's LX7186A switching regulator and LX8213 LDO
- Arduino and PMOD Connectors
- Push Buttons, DIP Switches, LEDs
- RJ45 Ethernet Connector
- Embedded FlashPro5
- USB for Power, UART and Debug
- Test Points

- Along with the SF2+ Development Kit hardware, three separate designs are delivered:
  - 90 K LE SmartFusion2 device
  - Low power application that features the Flash*Freeze capabilities of the SmartFusion2 SoC FPGA.
  - Audio application that features the Timberwolf audio processor to record and play back audio.
  - uClinux boot demo only

  Note the uClinux boot is demo only, source is not provided. Customers can access details from Emcraft directly:emcraft.com/products/255

Ordering Code	Supported Device	Price
SF2PLUS-DEV-KIT	M2S010-FG484	$125 available from ARROW

IGLOO2 Evaluation Kit
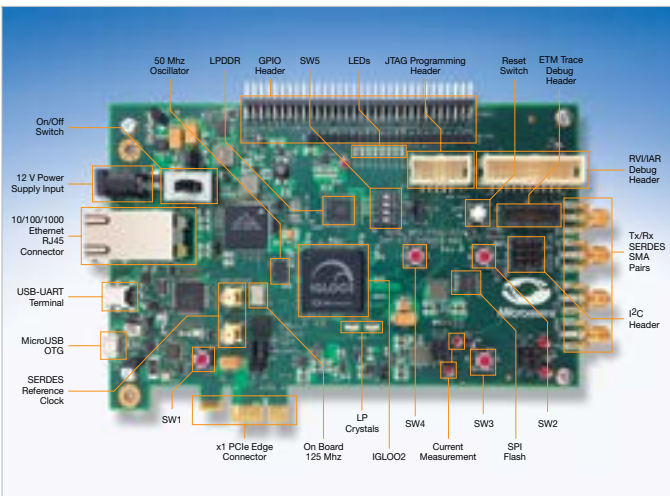
- Gives designers access to IGLOO2 FPGAs which offer leadership in I/O density, security, reliability and low-power into mainstream applications
- Supports industry-standard interfaces including Gigabit Ethernet, USB 2.0 OTG, SPI, I2C and UART
- Comes preloaded with a PCIe control plane demo
- Can be powered through a 12 V power supply or the PCIe connector and includes a FlashPro4 programmer
- Board features

- IGLOO2 FPGA in the FGG484 package (M2GL010T-1FGG484)
- JTAG/SPI programming interface
- Gigabit Ethernet PHY and RJ45 connector
- USB 2.0 OTG interface connector
- 1 GB LPDDR, 64 MB SPI Flash
- Headers for I2C, UART, SPI, GPIOs
- x1 Gen2 PCIe edge connector
- Tx/Rx/Clk SMP pairs

| Ordering Code	Supported Device	Price
M2GL-EVAL-KIT	M2GL010T-1FGG484	$ 399

Development Kits

DMPM Daughter Card
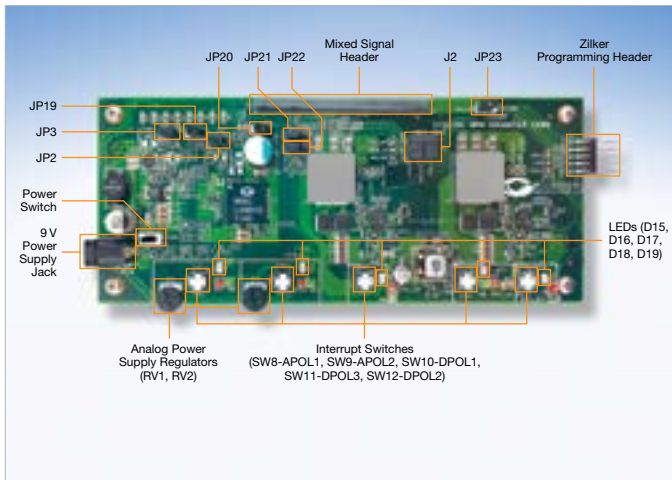
- Supports power management design with the SmartFusion Evaluation Kit and SmartFusion Development Kit
- MPM v5.0 design example implements configurable power management in SmartFusion SoC FPGA
- Graphical configuration dialog
- In-system reconfigurable
- 9 V power supply
- Board features

- 2 analog PoLs, 3 Digital PoLs
- 2 potentiometers to control analog regulators
- 5 power supply regulator interrupt switches
- 5 power supply regulator status LEDs
- Mixed signal header connector connects to SmartFusion board

ProASIC3 Starter Kit
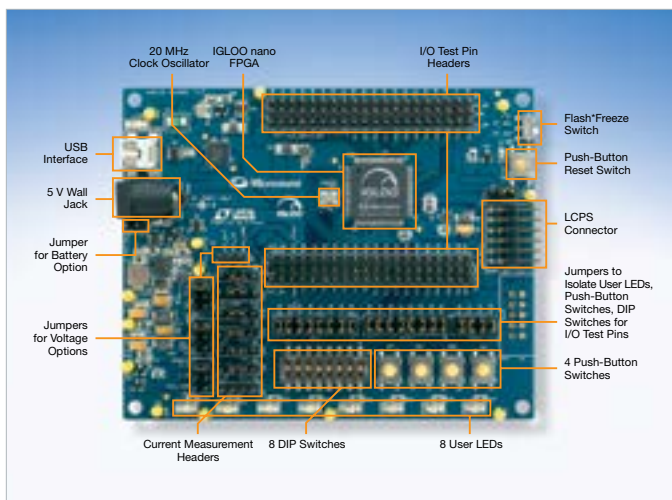
- Supports basic ProASIC3 FPGA design and LVDS I/O usage
- Free one-year Libero SoC software and Gold license
- FlashPro3 or FlashPro4 Programmer
- 9 V power supply and international adapters
- Kit user's guide, Libero SoC tutorial and design examples
- PCB schematics, layout files and BOM
- Board features

- Eight I/O banks with variety of voltage options
- Oscillator for system clock or manual clock option
- LEDs and switches for simple inputs and outputs
- LCD display module
- Two CAT5E RJ45 connectors for high-speed LVDS communications
- All I/Os available for external connections
- Not RoHS compliant

Ordering Code	Supported Device	Price
AGLN-NANO-KIT*	AGLN250V2-VQG100	$ 99

Note:
* Replaces -Z version of the nano Starter Kit.

ProASIC3 Starter Kit
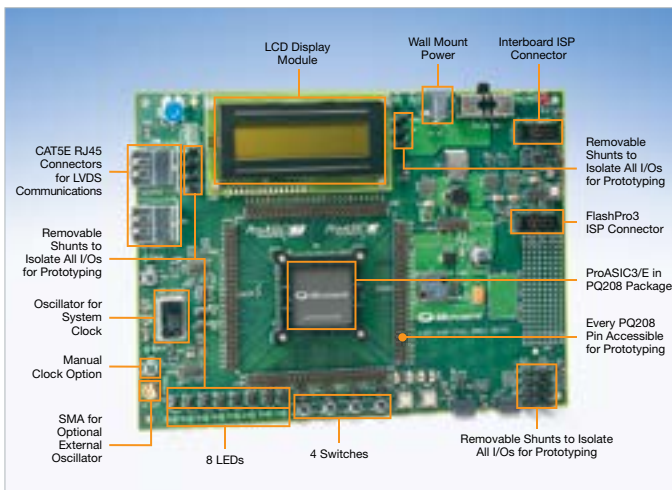
- Supports basic ProASIC3 FPGA design and LVDS I/O usage
- Free one-year Libero SoC software and Gold license
- FlashPro3 or FlashPro4 Programmer
- 9 V power supply and international adapters
- Kit user's guide, Libero SoC tutorial and design examples
- PCB schematics, layout files and BOM
- Board features

- Eight I/O banks with a variety of voltage options
- Oscillator for system clock or manual clock option
- LEDs and switches for simple inputs and outputs
- LCD display module
- Two CAT5E RJ45 connectors for high-speed LVDS communications
- All I/Os available for external connections
- Not RoHS compliant

Ordering Code	Supported Device	Price
A3PE-PROTO-KIT	A3PE1500-PQ208	$ 665

Development Kits

Core1553 Development Kit

Core1553-SA

Fusion Advanced Development Kit
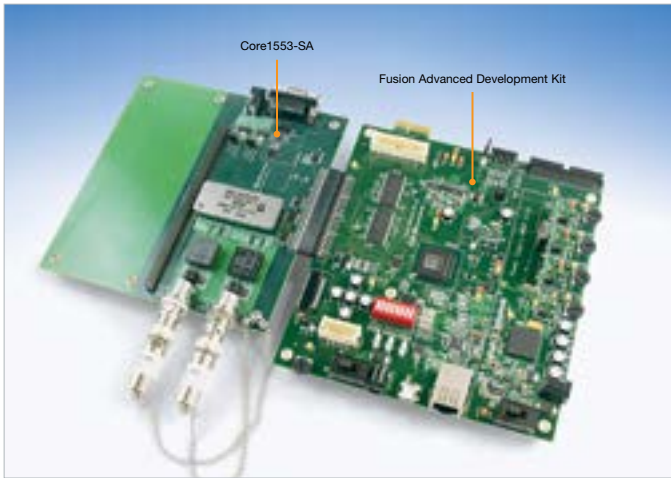
- Allows users to evaluate the functionality of Microsemi's Core1553BRM without having to create a complete MIL-STD-1553B compliant system
- Fusion Advanced Development Kit with two 9 V power supplies
- Core1553 daughter card
- User's guide, tutorial and design example
- PCB schematics, layout files and BOM
- Purchasing the kit gives the owner the right to the programming file of the demo, but not an evaluation of the IP. The IP evaluation or purchase is quoted separately.
- Board features

- MIL-STD-1553B transceiver, two transformers and two concentric twinax connectors included on the Core1553 daughter board
~ MIL-STD-1553B concentric twinax connectors are center pin signal high and cylindrical contact signal low
~ Connectivity is MIL-C-49142 compliant
~ Evaluate and develop medium speed on-board data communications bus solutions   for MIL-STD-1553B / UK DEF-STAN 00-18 (Pt.2) / NATO STANAG 3838 AVS / Avionic Standards Coordinating Committee Air-Std 50/2
- CAN bus interface support
- Connector to ARINC 429 Daughter Board (CORE429-SA)

Ordering Code	Description	Price
CORE1553-DEV-KIT	Core1553 Development Kit	$ 3,500
CORE1553-SA	Core1553 daughter card	$ 2,600

Additional Hardware Kits

Microsemi offers hardware choices for SoC FPGA and FPGA products. The table below lists additional popular kits available. Full details of these kits can also be found online with user's guides and accompanying tutorials.

Family	Ordering Code	Name	Device	Price	Power
SmartFusion	MPM-DC-KIT	MPM Daughter Card	None	$ 260	9 V
SmartFusion	MIXED-SIGNAL-DC	Mixed Signal Daughter Card	None	$ 65	N/A
SmartFusion	A2F-EVAL-KIT-2	SmartFusion Evaluation Kit	A2F200M3F-FGG484	$ 99	USB
Fusion	AFS-EVAL-KIT	Fusion Starter Kit	AFS600-FG256	$ 380	9 V
Fusion	M1AFS-ADV-DEV-KIT-PWR-2	Fusion Advanced Development Kit	M1AFS1500-FGG484	$ 820	9 V
Fusion	M1AFS-EMBEDDED-KIT-2	Fusion Embedded Development Kit	M1AFS1500-FGG484	$ 300	5 V
IGLOO	AGLN-NANO-KIT	IGLOO nano Starter Kit	AGLN250V2-ZVQG100	$ 99	USB
IGLOO	AGL-ICICLE-KIT	IGLOO Icicle Evaluation Kit	AGL125V2-QNG132	$ 150	USB
IGLOO	AGLP-EVAL-KIT	IGLOO PLUS Starter Kit	AGLP125V2-CSG289	$ 299	5 V
IGLOO	M1AGL1000-DEV-KIT	ARM Cortex-M1 IGLOO Development Kit	M1AGL1000V2-FGG484	$ 600	5 V
ProASIC3	M1A3PL-DEV-KIT	ARM Cortex-M1 ProASIC3L Development Kit	M1A3P1000L-FGG484	$ 600	5 V

Programming

Microsemi's solution makes programming and debugging easy, secured and convenient.

Programming Resources

- JTAG Programming
- SPI-Slave Programming

- MSS In-System-Programming (SoC FPGAs only)
- Auto Programming

- Auto Update
- In-Application-Programming (IAP)

FlashPro

The Microsemi FlashPro programming system is a combination of FlashPro software and hardware programmer. Together, they provide in-system programming (ISP) for the following families: IGLOO2, SmartFusion2, IGLOO Series, ProASIC3 series (including RT ProASIC3), SmartFusion, Fusion, ProASICPLUS, and ProASIC. For More information, refer to: http://www.microsemi.comproducts/fpga-soc/design-resources/programming/flashpro

FlashPro Programming Software

FlashPro Programming software comes bundled with the Libero SoC and is available for standalone download also. Programming software is available in two variants, FlashPro Software (Windows only) and FlashPro Express Software (Windows and Linux).

SiliconSculptor3

Silicon Sculptor 3 is an FPGA programming tool that delivers high data throughput and promotes ease of use, while lowering the overall cost of ownership.

Silicon Sculptor 3 includes a high-speed USB 2.0 interface that allows you to connect as many as 12 programmers to a single PC and uses a standalone software. Silicon Sculptor is an ideal solution for programming multiple high-density devices concurrently in the production environment.

For adapter modules, refer to:
http://www.microsemi.com/products/fpga-soc/design-resources/programming/silicon-sculptor-3

Programmer	Supported Device	Support	Price
FlashPro5	ProASIC3/E, ProASIC nano, IGLOO/e, IGLOO Plus, IGLOO nano, Fusion, SmartFusion, SmartFusion2, IGLOO2, RTProASIC3	• USB 2.0 • Windows and Linux	$ 49
FlashPro4	ProASIC3/E, ProASIC nano, IGLOO/e, IGLOO Plus, IGLOO nano, Fusion, SmartFusion, SmartFusion2, IGLOO2, RTProASIC3	• USB 2.0 • Windows	$ 49
FlashPro Lite	ProASICPLUS	• Parallel Port only • Windows • Software support until 9.1	$ 150
Silicon Sculptor III	All Flash and antifuse devices	• USB 2.0 • Windows	$ 3,960

DirectC / SPI-DirectC

DirectC and SPI-DirectC can be used for making minor modifications to the source code, adding the necessary Application Programming Interface (API), and compiling the source code and the API together to create a binary executable.

STAPL Player

The STAPL Player can be used to program ProASICPLUS, as well as third-generation flash devices such as SmartFusion2, IGLOO2, SmartFusion, IGLOO, ProASIC3, ProASIC3L, and Fusion, and interprets the contents of a STAPL file, which is generated by Microsemi's Libero SoC and IDE software tools. The STAPL Player reads the STAPL file and executes the file's programming instructions.
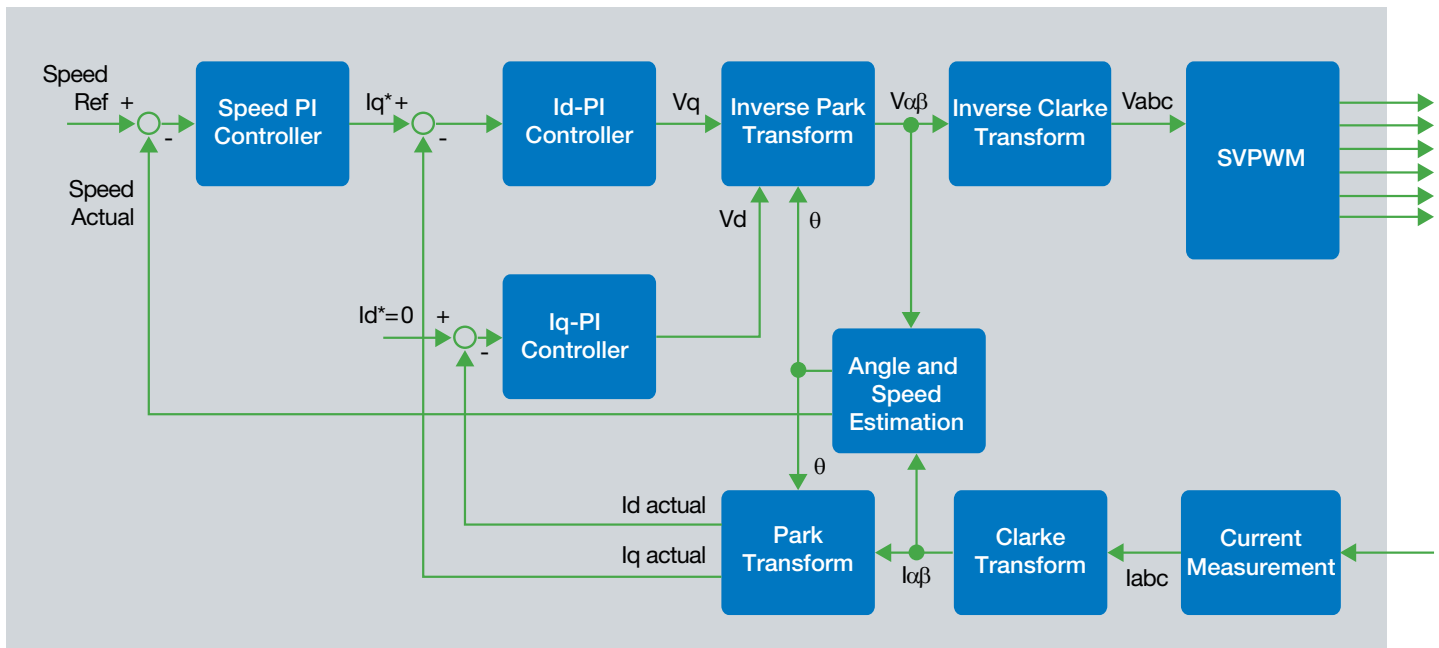
Motor Control Solution

Build Safe, Reliable Deterministic Motor Control Applications

Microsemi's Deterministic Motor Control Solution is specially designed to meet the challenging requirements of performance, reliability, and safety in an easy-to-use environment. The solution is compliant with industry coding standards for developing safe and reliable software for embedded applications. Microsemi offers a modular intellectual property (IP) portfolio, tools, reference designs, kits, and software to control motors such as permanent-magnet synchronous motor (PMSM)/brushless DC (BLDC) and stepper motors

Ordering Code	Supported Device	Price
SF2-MC-STARTER-KIT	M2S010-FG484	$ 799

Field Oriented Control - System Diagram

Reference Design Features

- Dual-axis deterministic motor control on a single system-on-chip (SoC) field programmable gate array (FPGA)

- Efficient, reliable, and safe drive/motor control with product longevity.

- A compact solution which saves board space and reduces product size.

- Motor performance is tested for speeds exceeding 100,000 RPM for sensorless field oriented control (FOC).

- Low latency of 1μs for FOC loop from ADC measurement to PWM enables switching frequencies up to 500 kHz.

- Design flexibility with modular IP suite.

- Has advanced safety features like "Automatic motor restart "and "Overcurrent protection".

- SoC integration of system functions to lower 'Total Cost of Ownership (TCO)'

Microsemi Intellectual Property

Microsemi enhances your design productivity by providing an extensive suite of proven and optimized (IP) Cores for use with Microsemi FPGAs and SoC FPGA and covers key markets and applications. IPs are organized as either Microsemi developed DirectCores or third party developed CompanionCores.

IP Cores are Searchable at: http://soc.microsemi.com/products/ip/search/default.aspx

Microsemi
***DirectCore*™**

Microsemi develops and supports DirectCore IP Cores for applications with the widest possible interest. Most DirectCores are available for free within our Libero tool suite. Common communications interfaces, peripherals and processing elements are all available as DirectCores. The list below shows examples of Microsemi's DirectCore offerings.

Functionality	DirectCore Examples
Connectivity	UART,16550, 429, PCI, JESD204B
DSP	CIC,FFT,FIR,CORDIC, RS
Memory Controller	FIFO, DDR, QDR, SDR, MemCtrl, MMC
Processor	Cortex-M3, 8051, 8051s, ARM7TDMI
Ethernet	MII, RGMII,GMII, SGMII
Security	DES, 3DES, AES, SHA
Error Correction	EDAC,RC

Microsemi
CompanionCore™

Microsemi CompanionCore Partners use their detailed system knowledge of common applications to craft optimized solutions targeted for Microsemi SoC FPGAs and FPGAs. CompanionCores are available for purchase from our partners and are easily integrated into your design using our Libero tool suite. The list below shows examples of CompanionCore Partners offerings.

Functionality	CompanionCores Examples
Connectivity	CAN, CANFD, PCIE, VME
DSP	FFT, JPEG, RS, DVBMOD
Memory Controller	SDRAMDDR, Flash, SD
Processor	80188, 80186, LEON3, 6809
Security	MD5, ARC4, RNG, ZUC, AES, SHA, 802.1ae (MACSec)
Error Correction	RS

Microsemi IP Available for Purchase for Use with Libero

Some Microsemi IP must be purchased separately as shown below. Please contact your local Microsemi Sales representative for information on price and licensing of Microsemi IP that require a separate license. CompanionCores supported by Microsemi are available at: http://www.microsemi.com/products/fpga-soc/design-resources/ip-cores#companioncores.

Product Number	Obfuscated RTL Available for Purchase	RTL Source Available for Purchase
CoreFFT	Not available	RTL source
Core1553BRM	Obfuscated RTL	RTL source
Core1553BRT, Core1553BRT_APB	Obfuscated RTL	RTL source
Core429, Core429_APB	Obfuscated RTL	RTL source
CorePCIF, CorePCIF_AHB	Obfuscated RTL	RTL source
CoreTSE, CoreTSE_AHB	Obfuscated RTL	RTL source
CoreCIC	Not available	RTL source

Notes:
1. Additional cores and configurations can be found on the website and in core handbooks.

High Speed Serial Interfaces

The high-speed serial interface solution comprises configurable functional blocks, IPs and reference designs. The high-speed serial interface block in SmartFusion2 and IGLOO2 product families, also known as Serializer/De-serializer (SERDES) integrates several functional blocks to support multiple protocols like PCIe, Ethernet, XAUI and EPCS.

- Gen1/Gen2 rates at x1, x2 and x4 links.
- Endpoint topology.
- Single-Function/Single-VC.
- Receiver and transmit buffers support error correction and coding (ECC).
- Fabric interface options of AXI3 Master/Slave or AHB32 Master/Slave.
- Address translation window support between PCIe and local device address space.

For more information on SERDES solutions, refer to http://www.microsemi.com/products/fpga-soc/technology-solutions/serdes-pci-express#overview.

PCIe

Microsemi offers implementation of PCIe protocol using the high-speed SERDES blocks. These blocks provide a fully hardened PCIe endpoint implementation, in compliance with the PCIe base specification revisions 1.1 and 2.0.

- Data rates ranging from 1 Gbps to 5 Gbps per lane.
- Supports 16 lanes at up to 5 Gbps each.
- 2 different reference clocks per SERDES block with 4 lanes each.
- Embedded PRBS generation/checking, debug and loopback functions supported with the SmartD**ebug module of Libero SoC.**
- User programmable emphasis and continuous time linear equalization.
- Data rates lower than 1 Gbps supported with a 3X oversampling reference design.

For more information on PCIe solution, refer to http://www.microsemi.com/products/fpga-soc/technology-solutions/serdes-pci-express#pci-express.

Ethernet

IEEE 802.3 specified high data rates are supported using the embedded Ethernet MAC and PCS layer of the MSS and soft IP blocks. Reference designs and application notes enable rapid development of SGMII, GMII, and XAUI protocols.

- Support for 10 / 100 / 1000 Mbps up to 100 Gbps
- Embedded XAUI block as part of the SERDES block
- Microcontroller Subsystem (MSS) Ethernet MAC – fully embedded MAC with SGMII or GMII physical layer interface

For more information on Ethernet solutions, refer to http://www.microsemi.com/products/fpga-soc/technology-solutions/serdes-pci-express#ethernet.

JESD204B

A complete solution for implementing the JEDEC JESD204B serial interface standard is available to interface external data converters using the SERDES blocks. CoreJESD204BTX (Transmitter) can be used to interface to digital-to-analog convertors and JESD204BRX (Receiver) can be used to interface to analog-to-digital convertors. Rx and Tx IP cores support data rates up to 3.2 Gbps at link widths of x1, x2 and x4. The cores can be reconfigured through the APB interface to allow EPCS mode achieve a higher data rate.

- Enables interfacing JESD204B compliant ADC/DAC convertors.
- Supports x1, x2 or x4 lanes.
- Performs word alignment and 8B/10B decoding and encoding.
- Recovers link configuration parameters and sources it with user selected parameter values during the initial lane synchronization sequence.
- Lane alignment sequence generation, buffering, monitoring and correction.
- Performs user-enabled frame alignment, monitoring and correction.
- Performs octet reconstruction, user-enabled descrambling/scrambling, alignment character generation and error detection.

For more information on JESD204B solution, refer to http://www.microsemi.com/products/fpga-soc/technology-solutions/serdes-pci- express#jesd204b

Microsemi is continually adding new products to its
industry-leading portfolio.

For the most recent updates to our product line and for detailed
information and specifications, please call, email or visit our website:

Toll-free: 800-713-4113

sales.support@microsemi.com

www.microsemi.com

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Sales: +1 (949) 380-6136
Fax: +1 (949) 215-4996
email: sales.support@microsemi.com
www.microsemi.com

Microsemi Corporation (Nasdaq: MSCC) offers a comprehensive portfolio of semiconductor and system solutions for communications, defense and security, aerospace and industrial markets. Products include high-performance and radiation-hardened analog mixed-signal integrated circuits, FPGAs, SoCs and ASICs; power management products; timing and synchronization devices and precise time solutions, setting the world's standard for time; voice processing devices; RF solutions; discrete components; security technologies and scalable anti-tamper products; Ethernet solutions; Power-over-Ethernet ICs and midspans; as well as custom design capabilities and services. Microsemi is headquartered in Aliso Viejo, Calif., and has approximately 3,600 employees globally. Learn more at www.microsemi.com.

MS2-004-15 55700049-06/02.16